27) **math coprocessor arithmetic and control instructions**

***Arithmetic instructions***

**FADD** ST (0) ST (0) +ST (1)

**FADD op** ST (0) ST (0) +”op” from memory or stack. Floating point operation.

**FADD op** ST (0) ST (0) +”op” from memory or stack. Integer operation.

**FADD ST (i), ST (0)** ST (i) ST (i) +ST (0); ST (0) popped

**FSUB** ST (0) ST (0) -ST (1)

**FSUB op** ST (0) ST (0) –„op” from memory or stack. Floating point operation.

**FSUB op** ST (0) ST (0) -“op” from memory or stack. Integer operation.

**FSUB ST (i), ST (0)** ST (i) ST (i) -ST (0); ST (0) popped

**FSUBR ST (i)** ST (i) ST (i) -ST (0) ; opposite instruction of FSUB ST (i)

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**FMUL** ST (0) ST (0) \* ST (1)

**FMUL op** ST (0) ST (0) \* ”op” from memory or stack. Floating point operation.

**FMUL op** ST (0) ST (0) x ”op” from memory or stack. Integer operation.

**FMULP ST (i), ST (0)** ST (i) ST (i) x ST (0); ST (0) popped

**FDIV** ST (0) ST (0): ST (1)

**FDIV op** ST (0) ST (0):”op” from memory or stack. Floating point operation.

**FDIV op** ST (0) ST (0):”op” from memory or stack. Integer operation.

**FDIVP ST (i), ST (0)** ST (i) ST (i): ST (0); ST (0) popped

**FDIVR ST (i)** ST (i) ST (i): ST (0);opposite instruction of FDIV ST (i).

**Command Instructions**

**FINIT** Initialization - the coprocessor is brought in an initial status known as ‘software reset’.

**FENI** accept interrupt

**FDISI** Ignore interrupt - this instruction ignores all interrupts regardless of the command register’s

bits;

**FLDCW adr** The command register is loaded from the memory location indicated by ‘adr’

**FSTCW adr** The command register is saved in a word located at the memory location

indicated by **‘**adr’

**FSTSW adr** The status register is saved in a word located at the memory location indicated

by **‘**adr’.

**FCLEX** The bits that define the exceptions are erased

**FSTENV adr** Save the environment - the coprocessor’s internal registers are saved in a

memory location starting at address ‘adr’ that has a size of 14 bytes.

**FLDENV adr** Load environment

**FSAVE adr** Save status - the coprocessor’s internal registers and its stack are saved in a memory

location starting at address ‘adr’ that has a size of 94 bytes.

**FRSTOR adr** Load status.

**FINCSTP** Increment stack pointer- after this instruction, the stack pointer is incremented with 1;

**FDECSTP** Decrement stack pointer

**FFREE ST (i)** Delete the ith element in the stack. The operation does not influence the stack pointer.

**FNOP** No operation.

**FWAIT** Waits for the current action to finish (similar to the 8086’s WAIT instruction)